R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to present a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals. The second circuit may be configured to present the one or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102 as being anticipated by Mullaney et al. '575 is respectfully traversed and should be withdrawn.

Mullaney discloses a high speed cross point switch routing circuit with a word-synchronous serial back plane (Title).

In contrast, the present invention provides a first circuit configured to present a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals. A second circuit may be configured to present the one or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

The so-called first circuit (elements 60 and 98 in FIG. 6 of Mullaney) does not appear to present one or more serial data signals to the so-called second circuit (elements 58 and 62 of Mullaney), as presently claimed. In particular, the output of the circuit 62 does not appear to be connected to the input of the circuit 86. The claimed first circuit is configured to respond to one or more serial data signals. The claimed second circuit is configured to generate "**said** one or more serial data signals". The serial data signals of the claimed first circuit provide antecedent basis for the claimed serial data of the second circuit. The Examiner points to the output of the element 86 as one or more serial data signals and the output of the serial converter 62 as serial data. Clearly these are not the same signals, even with the Examiner's interpretation. Therefore, Mullaney does not disclose or suggest each of the elements of the present claims. As such, the presently pending claims are fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, claims 17 and 19 provide that the first circuit responds to a plurality of serial data signals. The so-called first circuit (elements 60 and 98 of Mullaney) only responds to a single serial data signal. The so-called second circuit (element 62 and 96 of Mullaney) presents, at best, only a single serial data signal. In particular, the serial to parallel converter 60 in Mullaney was cited as part of the claimed first

circuit. However, claims 17 and 19 are directed to the second circuit. The explanation that the serial to parallel converter 60 receives one serial signal after another, does not appear to be relevant, since the converter 60 cannot be part of both the claimed first circuit and the claimed second circuit. As such, claims 17 and 19 are independently patentable over the cited reference and the rejection should be withdrawn.

Regarding claims 18 and 20, the parallel to serial converter 62 in Mullaney was cited as part of the claimed second circuit. However, claims 18 and 20 are now directed to the first circuit. The explanation that the serial converter 62 receives parallel signals once per processing cycle does not appear to be relevant. The converter 62 cannot be part of both the claimed first circuit and the claimed second circuit. As such, claims 18 and 20 are independently patentable over the cited reference and the rejection should be withdrawn.

In conclusion, Mullaney does not disclose or suggest a second circuit configured to present the one or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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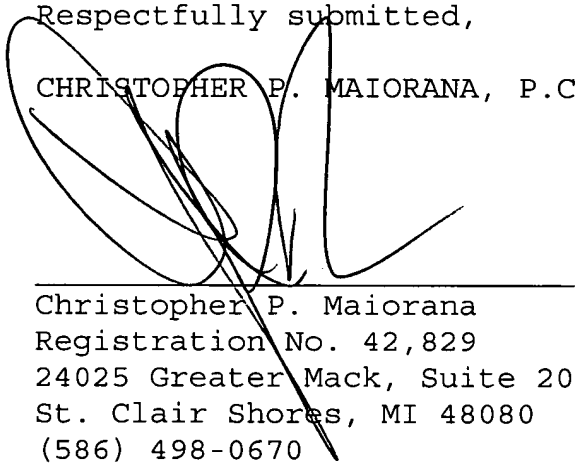

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Dated: May 29, 2003

Docket No.: 0325.00273